18

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,386	10/09/2003	Michael Norman Day	AUS920030132US1	8369

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EXAMINER	
MOAZZAMI, NASSER G	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/682,386	DAY ET AL.	
	Examiner	Art Unit	
	Nasser G. Moazzami	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/09/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Information Disclosure Statement submitted by applicant on 10/09/2003 has been considered by examiner. See attached PTO-1449.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Bauman (US Patent No. 6,587,931).

As per claims 1-8, AAPA discloses a first processor; a first cache associated with said first processor; one of a second processor or other device **[each of these processors have their own cache memory (page 1, lines 15-16)]**; and multiprocessor bus means connected to said first cache of said first processor and to said one of a second processor or other device for providing cache coherent communications via said bus means **[system bus]**; a second cache associated with said one of a second processor or other device and connected to said bus means a shared memory **[each of these processors have their own cache memory (page 1,**

lines 15-16)]; sending a request for a copy of system memory stored data to coherent memory configured caches of other devices, before attempting retrieval directly from system memory; storing data, retrieved from a cache associated with the requesting device **[offloading work to other processor (page 1, lines 11-12); the information may be retrieved from the other cache (page 1, lines 22-30)]**; and updating a state table associated with each coherent memory configured cache to reflect the appropriate state after the data is stored in the cache of the requesting device **[whether the state changes are required (page 1, lines 29-30); each cache in the system maintains a record of the cache state (page 2, lines 12-15)]**.

AAPA discloses the claimed invention, but fails to specifically teach that the first and second processors are non-homogeneous.

Bauman discloses a cache coherency system supporting multiple instruction processors **[column 4, lines 38-40]**, wherein the system is capable of supporting multiple heterogeneous instruction processors which allows the shared memory to be modified on other than strictly cache line boundaries **[column 3, lines 45-51 and column 5, lines 18-24]**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the current invention to use cache coherency for the multiprocessor as being taught by Bauman into AAPA multiprocessor system in order to allow the shared memory to be modified on other than strictly cache line boundaries.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Ediriosooriya (US Patent Application Publication No. 2004/0111563).

As per claims 1-8, Ediriossriya discloses a cache coherent memory system for use in a non-homogeneous multiprocessor system, comprising: a first processor **[processor 140 (Fig. 1)]**; a first cache associated with said first processor **[cache 142 (Fig. 1)]**; one of a second processor or other device non-homogeneous with said first processor **[processor 160 (Fig. 1); cache coherency between heterogeneous agents (Title)]**; and multiprocessor bus means connected to said first cache of said first processor and to said one of a second processor or other device non-homogeneous with said first processor for providing cache coherent communications via said bus means **[system bus 106 (Fig. 1)]**; and a second cache associated with said one of a second processor or other device non-homogeneous with said first processor and connected to said bus means **[cache 162 (Fig. 1)]**.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nasser G. Moazzami whose telephone number is (571) 272-4195. The examiner can normally be reached on 7:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NASSER MOAZZAMI
PRIMARY EXAMINER

12/02/2005